ATTACHMENT A

REMARKS

In response to the restriction requirement, Applicants provisionally elect Species I and Claims 1-5, without traverse. Claims 6-20 are withdrawn from consideration.

It is respectfully submitted that the claims are in an allowable form, and action to that end is hereby requested.

The Examiner is invited to call Applicants' attorney at the telephone number listed below in order to expedite prosecution of this application.

The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment, to **Deposit Account Number 07-1896,** and reference Attorney Docket **No. 351991-991320.**

Respectfully submitted,

DLA PIPER RUDNICK GRAY CARY US LLP

Date: 10/28/05

By: _____
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ATTACHMENT B

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.	:	~~10/822,944~~10/769,146
Applicant	:	~~Dana LEE, et al.~~Junichiro Watanabe
Filed	:	~~April 12, 2004~~January 29, 2004
TC/A.U.	:	~~2818~~2813
Examiner	:	~~Ngan NGO~~Tuan N. Nguyen
Title	:	~~ISOLATION LESS, CONTACT LESS ARRAY OF NONVOLATILE MEMORY CELLS EACH HAVING A FLOATING GATE FOR STORAGE OF CHARGES, AND METHODS OF MANUFACTURING, AND OPERATING THEREFOR~~SEMICONDUCTOR INTEGRATED CIRCUIT
Docket No.	:	~~351913-993000 (Previously 2102397-993000)~~351991-991320 (Previously 2102475-991320)
Customer No.	:	26379

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Maria Paula Kovacs

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO ~~OFFICE ACTION OF AUGUST 30, 2005~~RESTRICTION REQUIREMENT

Sir:

In response to the ~~Office Action~~**Restriction Requirement** dated ~~August 30~~September 29, 2005, please amend the above identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page ~~25~~8 of this paper.

~~2102397-993000~~

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ATTACHMENT B

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Original): A semiconductor integrated circuit comprising:

an internal circuit having first and second external terminals;

first and second fuse elements, each having first and second terminals, the first terminals of the first and second fuse elements being respectively connected to the first and second external terminals; and

a discharge line connected to the second terminals of the first and second fuse elements and serving as an electrostatic discharge current path.

Claim 2 (Original): The semiconductor integrated circuit according to Claim 1, wherein:

the internal circuit further has a MOS transistor having a gate connected to the first external terminal; and

each of the first and second fuse elements has a resistance value that satisfies:

$$V_{OX} > (R_m + R_x) \times I_{esd}$$

where V_{OX} represents a breakdown voltage of a gate oxide film of the MOS transistor, R_m represents a wire resistance value in the electrostatic discharge current path between the first and second external terminals, R_x represents a resistance value of all fuse elements arranged in the electrostatic discharge current path between the first and second external terminals, and I_{esd} represents a value of an electrostatic discharge current.

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Claim 3 (Original): The semiconductor integrated circuit according to Claim 1, wherein the fuse elements remain firm even when energy of 200μJ is applied thereto.

Claim 4 (Original): The semiconductor integrated circuit according to Claim 1, wherein the fuse elements remain firm even when energy of 200μJ is applied thereto but break when a direct current of 30mA is applied thereto within 20 seconds.

Claim 5 (Original): The semiconductor integrated circuit according to Claim 1, wherein the fuse elements are electrically disconnected when the semiconductor integrated circuit is mounted on a circuit board.

Claim 6 (Withdrawn): A semiconductor integrated circuit comprising:

an internal circuit having first and second external terminals;

an electrostatic protecting circuit connected to the second external terminal;

a fuse element having first and second terminals, the first terminal of the fuse element being connected to the first external terminal; and

a discharge line connected to the electrostatic protecting circuit and the second terminal of the fuse element and serving as an electrostatic discharge current path.

Claim 7 (Withdrawn): The semiconductor integrated circuit according to Claim 6, wherein:

the internal circuit further has a MOS transistor having a gate connected to the first external terminal; and

ATTACHMENT B

the fuse element has a resistance value that satisfies:

$$V_{OX} > (R_m + R_x) \times I_{esd}$$

where V_{OX} represents a breakdown voltage of a gate oxide film of the MOS transistor, R_m represents a wire resistance value in the electrostatic discharge current path between the first and second external terminals, R_x represents a resistance value of the fuse element, and I_{esd} represents a value of an electrostatic discharge current.

Claim 8 (Withdrawn): The semiconductor integrated circuit according to Claim 6, wherein the fuse element remains firm even when energy of 200μJ is applied thereto.

Claim 9 (Withdrawn): The semiconductor integrated circuit according to Claim 6, wherein the fuse element remains firm even when energy of 200μJ is applied thereto but breaks when a direct current of 30mA is applied thereto within 20 seconds.

Claim 10 (Withdrawn): The semiconductor integrated circuit according to Claim 6, wherein the fuse element is electrically disconnected when the semiconductor integrated circuit is mounted on a circuit board.

Claim 11 (Withdrawn): A semiconductor integrated circuit comprising:

an internal circuit having first, second and third external terminals;

a fuse element having first and second terminals, the first terminal of the fuse element being connected to the first external terminal;

ATTACHMENT B

first and second electrostatic protecting circuits respectively connected to the second and third external terminals;

a first discharge line connected to the first and second electrostatic protecting circuits and serving as an electrostatic discharge current path; and

a second discharge line connected to the second terminal of the fuse element and the second external terminal and provided to keep the first and second external terminals at substantially the same potential.

Claim 12 (Withdrawn): The semiconductor integrated circuit according to Claim 11, wherein:

the internal circuit further has a MOS transistor having a gate connected to the first external terminal; and

the fuse element has a resistance value that satisfies:

$$V_{OX} > (R_m+R_x) \times I_{esd}$$

where V_{OX} represents a breakdown voltage of a gate oxide film of the MOS transistor, R_m represents a wire resistance value in the electrostatic discharge current path between the first and second external terminals or between the first and third external terminals, R_x represents a resistance value of the fuse element, and I_{esd} represents a value of an electrostatic discharge current.

Claim 13 (Withdrawn): The semiconductor integrated circuit according to Claim 11, wherein the fuse element remains firm even when energy of 200μJ is applied thereto.

ATTACHMENT B

Claim 14 (Withdrawn): The semiconductor integrated circuit according to Claim 11, wherein the fuse element remains firm even when energy of 200μJ is applied thereto but breaks when a direct current of 30mA is applied thereto within 20 seconds.

Claim 15 (Withdrawn): The semiconductor integrated circuit according to Claim 11, wherein the fuse element is electrically disconnected when the semiconductor integrated circuit is mounted on a circuit board.

Claim 16 (Withdrawn): A semiconductor integrated circuit comprising:

a digital circuit having a first external terminal;

a first electrostatic protecting circuit connected to the first external terminal;

a first discharge line connected to the first electrostatic protecting circuit and serving as an electrostatic discharge current path;

an analog circuit having a second external terminal;

a second electrostatic protecting circuit connected to the second external circuit;

a second discharge line connected to the second electrostatic protecting circuit and serving as an electrostatic discharge current path; and

a fuse element connected between the first and second discharge lines and serving as an electrostatic current path of the digital and analog circuits.

Claim 17 (Withdrawn): The semiconductor integrated circuit according to Claim 16, wherein:

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the digital circuit further has a MOS transistor having a gate connected to the first external terminal; and

the fuse element has a resistance value that satisfies:

$$V_{ox} > (R_m+R_x) \times I_{esd}$$

where V_{ox} represents a breakdown voltage of a gate oxide film of the MOS transistor, R_m represents a wire resistance value in the electrostatic discharge current path between the first and second external terminals, R_x represents a resistance value of the fuse element, and I_{esd} represents a value of an electrostatic discharge current.

Claim 18 (Withdrawn): The semiconductor integrated circuit according to Claim 16, wherein the fuse element remains firm even when energy of 200μJ is applied thereto.

Claim 19 (Withdrawn): The semiconductor integrated circuit according to Claim 16, wherein the fuse element remains firm even when energy of 200μJ is applied thereto but breaks when a direct current of 30mA is applied thereto within 20 seconds.

Claim 20 (Withdrawn): The semiconductor integrated circuit according to Claim 16, wherein the fuse element is electrically disconnected when the semiconductor integrated circuit is mounted on a circuit board.

ATTACHMENT B

Application No.: 10/769,146
Attorney Docket No.: 351991-991320
Response to Restriction Requirement ~~Office Action of Sept. 29, 2005~~

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Respectfully submitted,

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